REMARKS

The present remarks are in response to the office action entered in the above identified case and mailed on April 20, 2004. Claims 11-20 are pending in the application. Claim 14 was amended only to correct a typing error. Claims 11 and 20 were rejected under 35 U.S.C. §112, second paragraph. The amended claims address this rejection. Claims 11, 12 and 15-20 were rejected under 35 U.S.C. §102(b) and claims 13 and 14 were rejected under 35 U.S.C. §103, all in light of the disclosure of Yamada et al. in U.S. Patent No. 5,412,655. Applicants respectfully traverse.

Yamada does not disclose, teach, or suggest all of the elements in any of the currently pending claims. Accordingly, the pending claims are neither anticipated by nor obvious over Yamada.

Claims 11 and 20 are the only independent claims pending in the instant application. As discussed in applicant's previous response, each of these claims calls for, among other things, a control signal sequence having a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals. Yamada's disclosure differs from the subject matter of Claims 11 and 20 because Yamada does not disclose, teach, or suggest a control signal sequence having a clock rate corresponding to the overall payload cell rate of N time-division multiplex communication terminals, wherein, the signals in the control signal sequence take on a first state or a second state, and wherein ATM cells are transmitted on demand to the N TDM terminals when the oldest control signal in the control signal sequence corresponds to the first state or a fixed data pattern is transmitted when the oldest control signal in the control signal sequence corresponds to the second state.

In the current office action the examiner summarizes Yamada column 5, lines 54-59, as "disclos[ing] a cell disassembly control unit 2, which controls the buffer memory, inherently comprising a clock rate that is compatible with the TDM data highway 11 and controls the transmission of cells or idle traffic corresponding to the overall cell rate of the nodes that transmit the TDM data" (See Office Action, pg. 8). Yamada does not inherently disclose this. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In Re Rijckaert 9 F.3d 1531, 1534, 28 USPQ2d 1955 (Fed. Cir. 1993) MPEP §2112. In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the

determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art. Ex Parte Levy 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990), MPEP §2112. In the present case, there are any number of ways to determine when cells are present, disassemble the cells and transmit the data. It is not necessary and inevitable, and thus not inherent, that a disassembly control unit have a control signal sequence having a clock rate corresponding to the overall payload cell rate of N time-division multiplex communication terminals, wherein, the control signal sequence takes on a first state or a second state, and wherein ATM cells are transmitted on demand to the N TDM terminals when the oldest control signal in the control signal sequence corresponds to a first state or a fixed data pattern is transmitted when the oldest control signal in the control signal sequence corresponds to a second state.

The section of Yamada the examiner points to for this inherency argument continues on to disclose that the TDM data is transmitted through the clock converter 10 to the TDM data highway 11 (See column 5, lines 59-61). The clock converter is disclosed in Yamada such that, the TDM data is transferred from the internal clock to the clock of TDM data highway 11 by the clock converter 10, and is transmitted to the TDM data highway 11 (See column 6, lines 26-28). This passage teaches nothing regarding a control signal sequence having a clock rate corresponding to the overall cell rate of the TDM data highway. The clock rate of the TDM data highway affects the overall cell rate of the TDM data highway, but the two are not the same.

Furthermore, Yamada column 5, lines 54-59 states that the cell disassembly unit controls the buffer memory and the address memories "such that data is read out from the bank storing the payload data in units of the TDM fixed bit rate data for each virtual channel specified on the basis of the frame pulse and clock of the TDM data highway." Thus, data are read out of the buffer memory according to the TDM data highway bit rate and according to the TDM data highway frame structure. Again, this is not the same as a control signal sequence having a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals.

The Examiner interprets the control signal generated by the cell disassembly unit, which controls whether cells or idle data are transmitted to the TDM data highway, as inherently representing a status for each transmission, and as the "oldest" control signal sequence. True, the output of the cell disassembly control unit performs a similar function as the control signal

sequence of the present invention, namely determining whether actual cell data or idle data will be transmitted to a TDM terminal, but there is no teaching how this output signal is generated. There are many possibilities. Most importantly, it is not necessary that the output of the cell disassembly unit be derived from a control signal sequence having a clock rate equal to the overall cell rate of the TDM data highway. This is especially true due to the differences in the way cell payload data is handled in the present invention versus how they are handled by Yamada. In the present invention cell payloads are stored in a queue in the order they are received, whereas, Yamada maintains an elaborate system for maintaining the addresses of the first and last of the cells received as well as a time series chain of arrival time relationships of the cells from the first to last. It is not difficult to imagine Yamada basing the decision to transmit cell data or idle data from the buffer memory on some criteria other than a control signal sequence having a clock rate corresponding to the TDM data highway. For example, Yamada could track the address of the last cell transmitted and so long as the last transmitted cell address does not equal the last cell address, cell data from the buffer memory is transmitted. When the last transmitted cell address equals the last cell address, then Yamada could decide to transmit idle data. Thus, the control signal sequence having a clock rate corresponding to the overall cell rate, CR_N, of N TDM terminals of the present claims is in no way inherent in the disclosure of Yamada.

Finally, Yamada discloses transmitting data to a singular "TDM data highway 11". Yamada does not disclose transmitting ATM cells on demand to N multiple TDM terminals. Thus, Yamada in no way indicates having a control signal sequence with a clock rate corresponding to the overall payload cell rate CR_N of N time-division multiplex communication terminals.

Since Yamada does not disclose, teach or suggest explicitly or inherently all of the features of the independent claims pending in the present application, the rejections under 35 U.S.C. §102(b) are improper and should be withdrawn. The dependent claims are allowable for the same reasons.

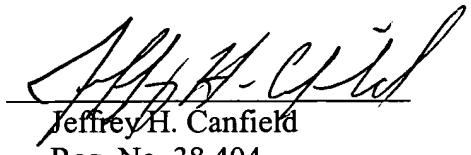
For these reasons, Applicant respectfully submits that the claims as they presently stand are all in condition for allowance. Applicant therefore requests that the Examiner allow the claims and move the application to issue. However, if there are any remaining issues the

Examiner is encouraged to call Applicant's attorney, Jeffrey H. Canfield at (312) 807-4233 in order to facilitate a speedy disposition of the present case.

If any additional fees are required in connection with this response they may be charged to deposit account no. 02-1818.

Respectfully submitted,

BELL, BOYD & LLOYD LLC

BY 

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